

μ PC8240T6N-EVAL-A

Evaluation Board

- Circuit Description
- Performance specifications
- S-parameter plots
- Circuit schematic and assembly drawing

Circuit Description

Matching Circuits

C2 is used for both DC block and output matching. It should be placed close to the device.

The input matching is mainly realized by L1. A high Q wire-wound type inductor is used on this board which slightly improves noise figure. The value of L1 is chosen for a reasonable balance between input return loss and noise figure. The input return can be improved, at the expense of noise figure, by lowering the value of L1.

PCB Material

The PCB is FR4 four layer board. The top and bottom dielectric layers are 8mil thick. The total board thickness is 62mil.

Typical Performance Specifications

Test Conditions:

$f=1575\text{MHz}$; $V_{cc}=V_{ps}=2.7\text{V}$

Noise Figure: 1.1dB (direct measurement on board, no subtraction of board loss)

Gain: 27dB

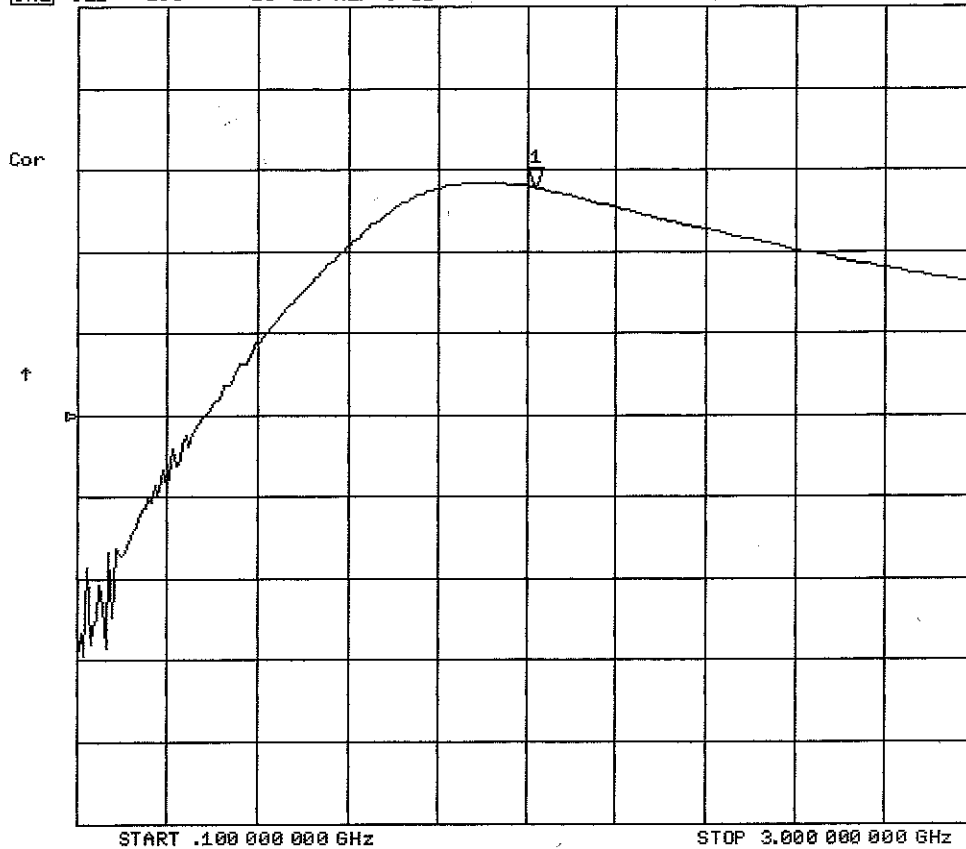
Input return loss: -10dB

Output return loss: -15dB

Gain and return loss plots over wider frequency range are shown on the next page.

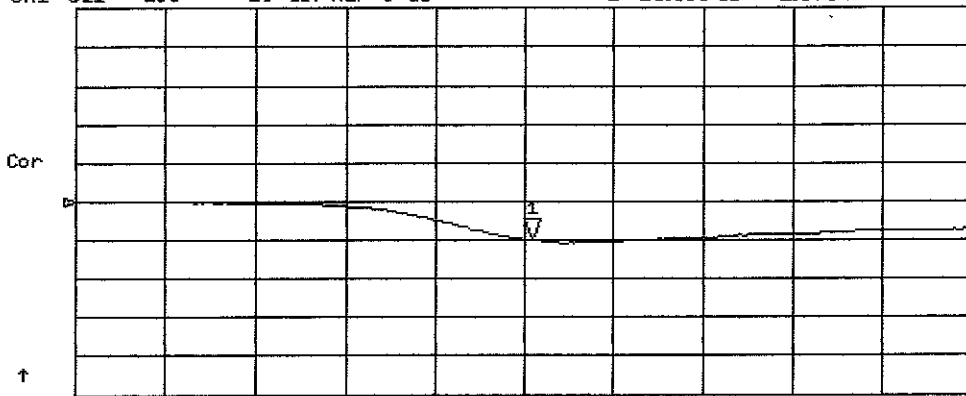
22 May 2009 14:53:33

CH1 S21 LOG 10 dB/REF 0 dB 1: 27.790 dB 1.575 000 000 GHz

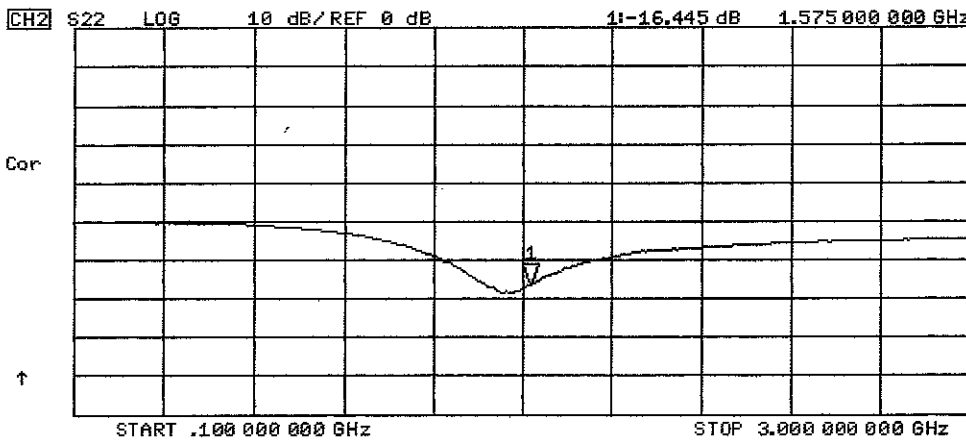


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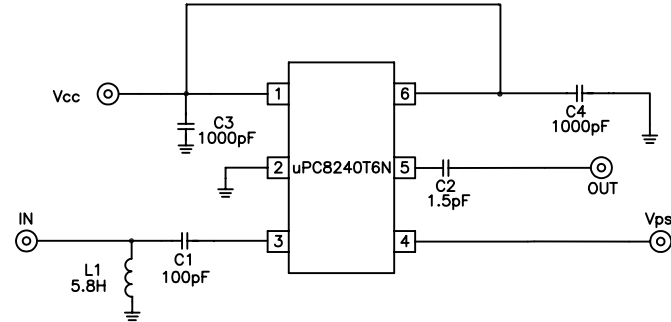
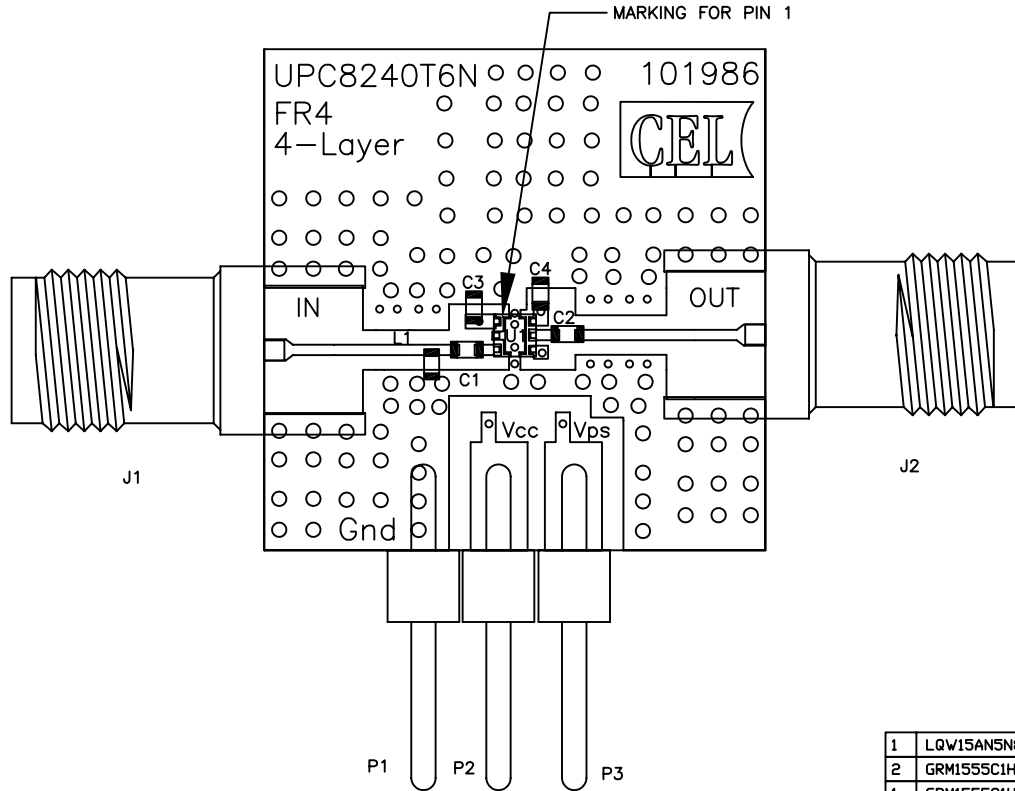
CH1 S11 LOG 10 dB/REF 0 dB 1: -10.066 dB 1.575 000 000 GHz



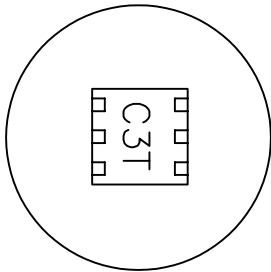
CH2 S22 LOG 10 dB/REF 0 dB 1: -16.445 dB 1.575 000 000 GHz



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



1	LQW15AN5N8G00	L1	0402 5.8nH IND MURATA WIREWOUND	8
2	GRM1555C1H102JA01D	C3,C4	0402 1000pF CAP MURATA	7
1	GRM1555C1H1R5CZ01D	C2	0402 1.5pF CAP MURATA	6
1	GRM1555C1H101JZ01D	C1	0402 100pF CAP MURATA	5
3	2340-6111 TG	P1,P2,P3	PIN HEADER 3M	4
2	142-0711-821	J1,J2	SMA FEMALE CONNECTOR E.F.JOHNSON	3
1	uPC8240T6N	U1	NEC uPC8240T6N	2
1	CL-101986	DRAWING	COMPONENT LAYOUT DRAWING	1
QTY	PART NUMBER OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION	ITEM NO.



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES	
DECIMALS	ANGULAR
.XX±	±
.XXX±	
DO NOT SCALE DRAWING	
MATERIAL	
FINISH	
NEXT ASSY	USED ON
APPLICATION	

APPROVALS	
Drawing by:	01/13/2009
Designed by:	01/13/2009
Checked by:	
Project Engineer:	
Quality Control:	

CALIFORNIA EASTERN LABS 4590 PATRICK HENRY DR. SANTA CLARA CA. 95054			
TITLE: uPC8240T6N-EVAL-A ASSEMBLY DRAWING			
SIZE	FSCM NO.	DWG NO.	REV
C		AD-101986	-
SCALE	RELEASE DATE	PROTOTYPE	SHEET 1 OF 1